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A Novel Approach to Build a Gated Integrator for High-Resolution Energy Spectroscopy Systems

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Abstract: *A gated integrator (GI) is to solve the ballistic deficit problem by integrating the signal until all the charge is collected from the detector. With the development of radioactive ion beam physics, heavy-charged particles like carbon ions have been applied to the treatment of deep-seated inoperable tumors in the therapy terminal of the Heavy ion Research Facility in Lanzhou (HIRFL) located at the Institute of Modern Physics (IMP), Chinese Academy of Sciences (CAS). An accurate low current measurement circuit was developed to control the beam current at 1pA range. The circuit consisted of a low current high sensitivity I/V converter and GI in an energy spectroscopy. This paper will show a new switch configuration made by transmission gates circuit which is used to prevent leakage current and at the same time used as a novel technique to compensate a charge injection in the reset switch.*

Keywords: *Energy spectroscopy; Gated integrator; Transmission gates; Charge injection; Switch; Leakage current; Noise*

I. Introduction

The development of imaging systems such as Schottky-barrier detector (SBD), CMOS APS (complementary metal-oxide field effect transistor active pixel sensor), Si CCD (charge coupled device), InGaAs, InSb, and HgCdTe FPAs are all based on the concept of current integration to accumulate signal in the purpose of improving the SNR (signal-to-noise ratio), dynamic range and sensitivity**.** In CSR IMP Lanzhou, the main works are heavy ion beam accumulation, experiments related to cancer therapy, patients' treatment, mass measurement and prophase experiments on recombination [1, 3]. One of the main functions of electron cooler in CSR was heavy ion beam accumulation. The accumulation efficiency functioned with a lot of parameters of storage ring and electron cooler, such as electron density, the work-point setting, closed-orbit, and angle between electron beam and ion beam. When the experimental started, the electron beam alignment was done to maximize the accumulated ion beam intensity. Since the year 2006, up to today, a number of patients have been irradiated in the therapy terminal of the heavy ion research facility in Lanzhou (HIRFL) at IMP, where carbon-ion beams with energies around *100 MeV/μ* can be supplied and a passive beam delivery system has been developed and commissioned [4]. Many therapeutic and clinical experiences concerning heavy-ion therapy have been acquired at IMP. To develop and exploit the heavy-ion therapy project to deep-seated tumor treatment, a system such as a horizontal beam line dedicated to this has been built in the cooling storage ring (CSR), which is a synchrotron attached to the HIRFL as an injector to be analyzed by detectors, and is now in operation. A beam current monitor (BCM) was also needed to calibrate these detectors. Beams applied to treatment are smaller than *1pA*. These low beams current are modulated because of operating modes of a synchrotron and also suffer from poor quality system [2, 5].

This paper presents a description of a low current measurement circuit for high-resolution energy spectroscopy systems. In detail the paper will describe the structure of GI based on leakage current, charge injection, noise analysis and introduction of a switch technique with high sensitivity when comes the measurement of low current. It also shows that the noise analysis during a transient voltage excursion appeared at the gate can sense the readout system.

II. Gated Integrator For High-Resolution

Fig.1. Shows the block of the heavy ion beam current monitor system. The accurate current measurement circuit consists of I/V Converter and a GI. The current signal from the Faraday cup (FC), which was pulsed for *0.5ms* a period of *4ms*, was converted into a voltage signal through a I/V Converter, the output of which was integrated by the GI in order to measure the charge of the beam [2], [6]. Outputs of I/V Converter and GI were acquired by a data acquisition system based on PXI. The signals were processed by the local computer. Compared to former current gated integrators [2], [7], which integrated the current from the FC by a GI directly, the new circuit prevent against many disturbances like leakage charge injection of switches, current of the feedback capacitor and the noise during a transient voltage excursion.

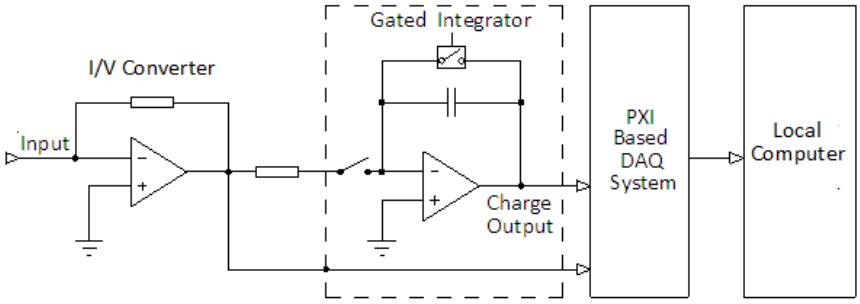

Fig.1. Block diagram for high-resolution energy spectroscopy systems

III. The Design Of The Novel GI

A gated integrator is designed to receive and recover fast, repetitive, analog signals with time scales ranging from 10^{-11} to 10^{-4} seconds. In a typical application, a time window within a certain width is "gated" after a set delay from an internal or external trigger. A gated integrator stands to amplify and integrate the signal that is present during the time the gate is open, excluding noise and interference that may be present at other times. The gated integrator is actually a capacitive transimpedance amplifier (CTIA) except the gated switch, so it also performs as a low pass filter. To receive the total charge of the beam, the output of the (I/V) converter was fed into the GI, the schematic indicated by the dotted line in Fig. 1. The input signal voltage U_i is converted into current through the resistor R_S and integrated by the feedback capacitor C_f. The output voltage U_{out} is given by

$$U_{out} = \frac{1}{R_S C_f}\int_0^T U_i(t)dt + \delta_0 \qquad (1)$$

where U_i is the input voltage, proportional to the current from the (I/V) converter, U_{out} is the GI output voltage, which represents the total charge of the beam for a given duration T and δ_0 is the initial voltage in the feedback capacitor of the GI. The leakage current elimination techniques and charge injection compensation were implemented in the GI section. The GI circuitry is composed of switches, operational amplifier and capacitors. The non-ideal switch and amplifier will introduce additional noise and fixed pattern [8, 9]. The goal of the design is trying to understand the issues and take appropriate strategies to limit them such that the performance of the circuitry is not overshadowed.

3-1 Characteristics of MOS as a switch

The main features of a MOS switch are charge injection, switch speed, and clock feedthrough. The rise and fall times of a submicron gate switch is usually less than *0.1 ns*. This can impose a problem only in readout circuit of extremely high speed FPAs (Focal Plane Array). The charge injection and clock feedthrough, however, are the main sources of noises in a MOS switch.

3-2 Switch configuration to prevent leakage current

A MOS switch configuration as a switch is used to pass voltage or current. An ideal switch has the characteristics of zero resistance when it is ON, infinite resistance when it is OFF and no delay when it is turned ON or OFF. A real MOS switch however, has turn-ON non-zero channel resistance, turn-OFF leakage current, parasitic capacitances and threshold voltage.

While the GI is in integration state, the effect reset switch has to be kept OFF. However the effect of leakage current in the GI reset switch will induce errors to the output in the long duration of these states. The problem can be resolved by using the MOS switch configuration to substitute single reset switch shown in fig. 2.

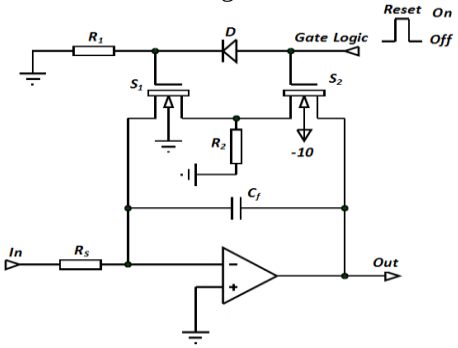

Fig. 2 A MOS switch configuration as the reset switch.

Although both NMOS integrator, are switched at the same time, S_1 is switched with gate voltages of *0* and *5V* so that gate leakage is totally eliminated during the OFF state. In the ON state the capacitor is discharged now with twice R_{ON}. In the OFF state, a very small leakage passes through S_2 to ground via R_2 with little drop. Then there is no leakage current at the summing junction because S_1's source, drain, and substrate are all at the same voltage. If the body and source are at the same potential, the drain to source current of a MOS transistor in the deep sub-threshold region of operation is given by

$$I_{DS} = KI_{DO} \cdot \exp\left(\frac{V_{GS} - V_{th}}{\eta V_T}\right)\left(1 - \exp\left(-\frac{V_{DS}}{V_T}\right)\right) \tag{2}$$

$$I_{DO} = \mu_n C_{OX} (\eta - 1) V_T^2$$

where, I_{DS} is the drain to source current of the transistor MOS, K is the aspect ratio of the transistor, I_{DO} is the saturation current, V_{GS} is the gate to source voltage, V_{th} is the threshold voltage of a MOSFET, V_T is the thermal voltage, V_{DS} is the drain to source voltage, μ_n is the carrier mobility, C_{OX} is the gate oxide capacitance, and η is the sub-threshold slope factor [6], [7], [10]. Eq.(2) shows, even for $V_{GS}=0$, the true way to obtain a zero switch leakage current is to set V_{DS} to *0 V*. To maintain the V_{DS} of the MOS switch at zero, a switch configuration shown in Fig. 2 is used to substitute the single reset switch from the gate integrator in figure 1. The Switch configuration is composed of two MOS switches, S_1, S_2, in series and a grounded resistor, R_2, attached to the node between the two switches. When the two CMOS switches in parallel with the storage capacitor are OFF, a very small leakage passes through S_2 to ground via R_2 with little drop. Then there is no leakage current at the summing junction because S_1's source, drain, and substrate are all at the same voltage. Thus, in this switch configuration, V_{DS} of the switch attached to the inverting input of the integrator is maintained at virtual *0 V*, and zero or negligible leakage current passes through this switch circuit.

3.3. Charge injection prevention

When the MOS is ON, some charges are present under the gate oxide resulting from the inverted channel. When the switch turns OFF, part of these charges will be injected into the capacitor C_{int}. For a NMOS the charge under the gate can be estimated by

$$Q_{IN} = -C_{OX} WL(V_{GSN} - V_{THN}) \tag{3}$$

and for a PMOS the channel charge is

$$Q_{IP} = -C_{OX} WL(V_{GSP} - V_{THP}) \tag{4}$$

It is noted that the injection charges are negative for NMOS and positive for PMOS. The problem can be resolved by using a CMOS transmission gate switch to replace each NMOS in switch configuration. The CMOS transmission gate is composed of a NMOS and a PMOS connected in parallel controlled by complementary signals. Since it is known that the signs of the charges in an n-channel and in a p-channel in the equations (3) and (4) are opposite, the charges injected from the n-channel and the p-channel will cancel out each other if their areas of gates are carefully designed shown in fig. 3**.** A transmission gate, or analog switch, is defined as an electronic element that will selectively block or pass a signal level from the input to the output. This solid-state switch is comprised of a PMOS transistor and NMOS transistor. The control gates are biased in a complementary manner so that both transistors are either ON or OFF. As a switch a transmission gate, has turn-ON non-zero channel resistance which is better than the one of a single MOS switch.

As the charge injection induces two effects for the integrator. First it takes part of the storage well; the integrator must have a capacity that is much larger than the number of injected carrier. Second, the injected charge causes fixed pattern noise that is in the order of square root N_{IN}, which can fix the limit of minimum detectable signal. The first problem finds the solution by using a CMOS transmission gate switch. The second problem can be sort of suppressed if a slow change clock is used to turn OFF the switch. When the signal of the clock is slow, the charges in the channel will mostly be injected into the substrate. Without these solutions, when a transient voltage excursion appeared at the gate, there would be an injection of electric charge into analog path, which would cause errors to the GI output. After analysis and experimental trials, parameters were adjusted from the equations (3) and (4). Thus by adjusting also the amplitude of the voltage excursion, the error of the output voltage caused by charge injection was reduced to less than ***1.4mV.***

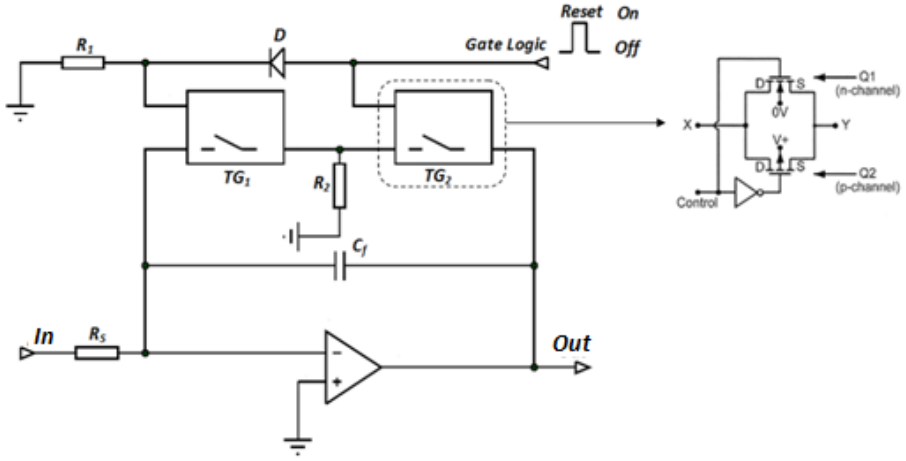

Fig.3. Schematics of the GI for charge injection compensation.

IV. Results And Discussion

The measurements were developed in the laboratory to know the DC and AC characteristics and the performances of the circuit. The streaming signal generator XLV1 associated with voltage controlled current source was selected to supply input current signal to the Gated Integrator on the software program PSPICE. Specification of the New GI is shown in table 1. Parameters were measured when the source current was in DC mode. The DC test results presented here, including linearity shown in fig.4.

Table 1: Specifications of the new GI.

Parameter	Value
Full scale output	±5V
Voltage conversion gain	-1.0 V/V
Linearity error	<0.06%
Output voltage noise	<1.4mV (rms)
Output offset voltage	<0.5mV(rms)
Injected charge	<116pC
Temperature range	-40 °C to 125°C

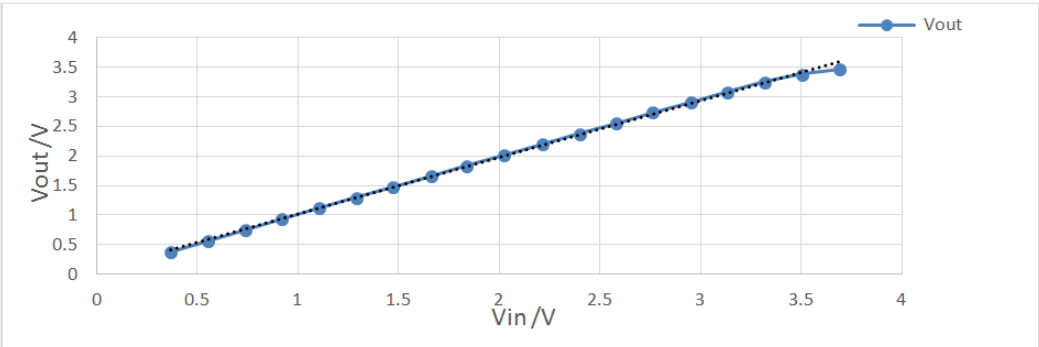

Fig. 4. Measured non-linearity of the GI.

In order to recover the signal from the measurement system, figure 5 shows how single switch does not prevent leakage current. Then it will be difficult to recover the entire signal. When we substitute a single reset switch by MOS switch configuration shown in figure 2, the leakage current disappear see figure 6, but we still remark an error appearance when the switch turns ON. This error is from the charge injection. During the rising edge of the clock signal of the gate, the gate starts at *0 V* and increases toward high voltage. In the transition from *0* to $V_{in}+V_{th}$, the switch is OFF. Consequently, this part of the clock waveform can couple to C_{int} via C_{GS}. As a result, a portion of the clock signal appears across C_{int} as indicated on the figure 6 during the transition at *3.8ms*. The problem will be resolved by using a CMOS transmission gate switch to substitute each NMOS in switch configuration see figure 7.

In contrary to charge injection when the switch is turned from ON to OFF, there is charge absorption when the switch is turned from OFF to ON for successive readout signal, which will cause an error too shown in figure 8, for second and third readout during a low current measurement. At this level, we can solve the problem by using a long channel transistor MOS (ancien technology) or use a slow change clock to turn OFF the switch,

see figure 9. These results because the charges in the channel will be mostly injected into the substrate before reach the end of the channel.

The injected charge induces fixed pattern noise, which will limit the minimum detectable signal. To choose a proper voltage for the clock signal of the gate to reduce pattern noise also, the analysis of noise effect is developed. The number of these charges varies with the voltage of the gate. They are shown in the figure 10. One can just find a difference among the figures 8, 9 and 11. The simulation results show how noise effect appears when we are measuring low values and disappear with slow change clock. This noise effect is also negligible or disappears when the measurement is substantial compare to low values.

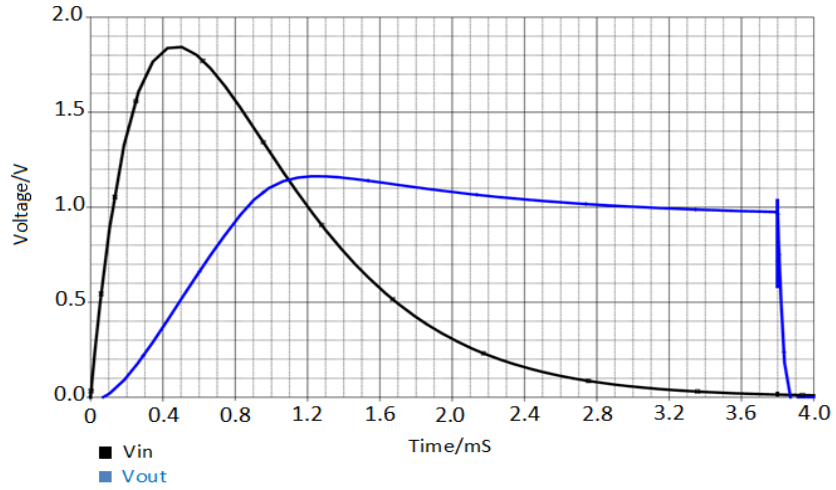

Fig. 5. Output waveform of the GI from I/V converter output using a single reset switch

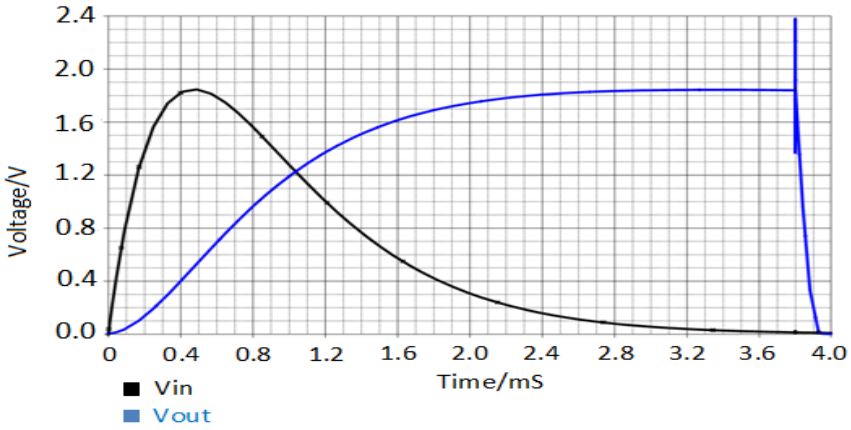

Fig. 6. Output waveform of the GI from I/V converter output using switch configuration made by two NMOSFETs

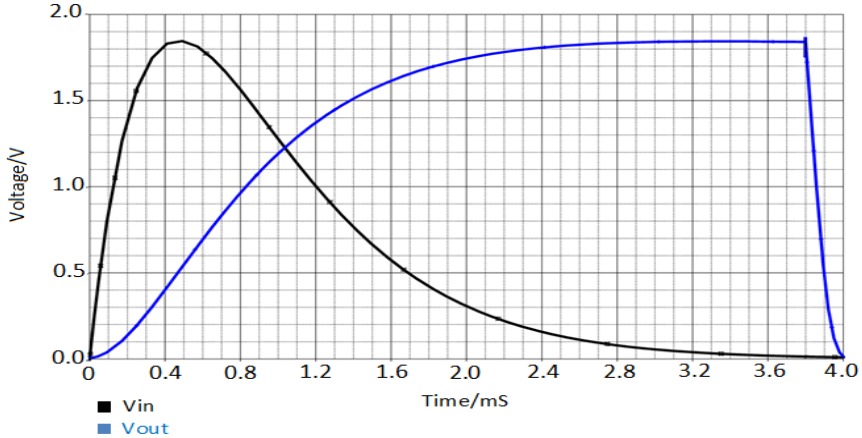

Fig 7. Output waveform of the GI from I/V converter output using switch configuration made by two transmission gates to prevent charge injection

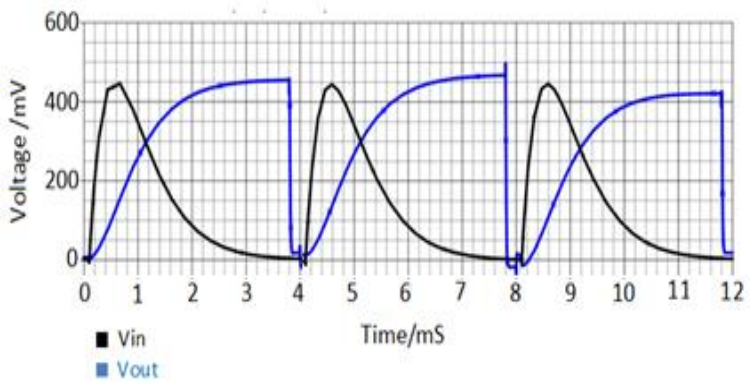

Fig. 8. Fast change clock to turn OFF the switch

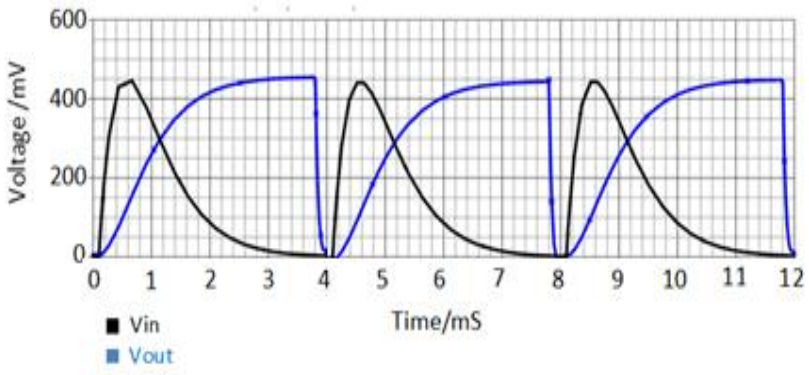

Fig. 9. Slow change clock to turn OFF the switch

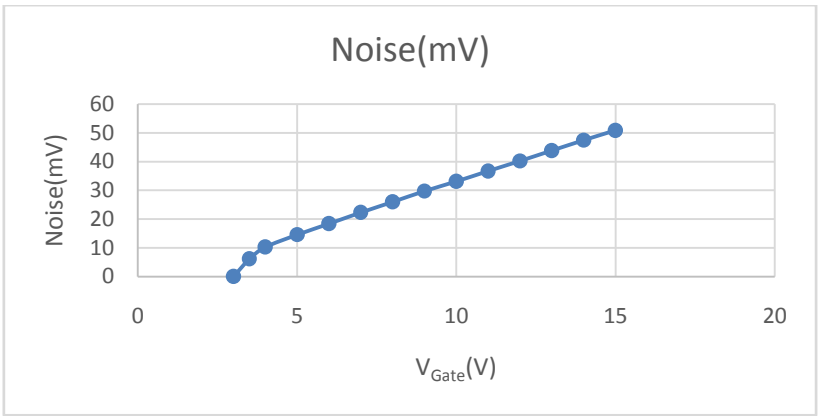

Fig. 10. Noise effect for the integrator versus clock voltage gate

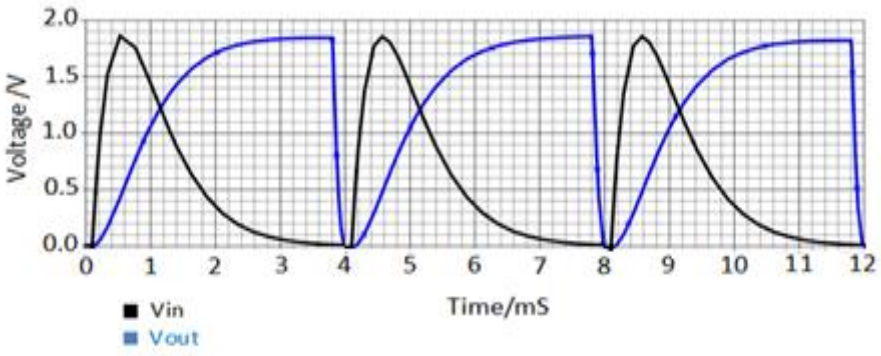

Fig. 11. Fast and slow change clock to turn OFF the switch with substantial value measurement

V. Conclusions

With the new designed circuit, computer simulation was carried out by PSPICE simulator. The high degree of linearity was achieved by using MOS switch configuration, used as a new technique to prevent leakage current and at the same time a novel compensation approach circuit which reduced the charge injection from switches in the GI to *1.4mV*. The results of the simulation show how noise effect appears when we are measuring low values and disappear with slow change clock**.** This noise effect is also negligible or disappears when the measurement is substantial. The results of the simulation of a low and medium current measurement circuit show that it had a high accuracy and stability. Because of the circuit design techniques used for high event rate capability insured that the circuit would perform well in high-resolution energy systems.

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